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LARGE FLIP CHIP ASSEMBLY CHALLENGES AND RISK MITIGATION PROCESS

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ABSTRACT

Next generation high speed network/communication packages require much larger die sizes and increased ball counts (>3000) to meet high speed, high input/output (I/O) functionality and improved reliability performance. Demand for such high speed large flip chip packages create an opportunity for highly integrated multi-chip modules (MCM's) and 2.5D/3D silicon (Si) interposer packages which are gradually emerging to meet these requirements. Achieving both increased margins in the power delivery network and increased functionality in next generation high speed network/communication applications requires extremely efficient, low loss package designs with body sizes 50X50mm or larger. One of the biggest challenges for such large die, large body packages is how effectively the assembly risk can be mitigated while fulfilling long term package reliability and functionality. The work presented in this paper describes key factors for mitigating several assembly related issues in the industry, including package warpage/co planarity, and the identification of the optimum processes and materials for successfully manufacturing large body flip chip packages with high assembly yields.

As the body sizes and die sizes increase, the chip-to-package interaction failure risk increases significantly due to a larger distance to neutral point (DNP). Typical assembly risks are extreme low-k (ELK) delamination (white bumps) during the chip joining process, bump tearing or cracking, underfill delamination, and warpage issues. A comprehensive experiment was carried out to achieve the objective of the work. A test vehicle was developed using a 21x22mm^2, flip chip copper (Cu) column bumped die placed onto a 50x50mm body size, using a multi-layer substrate with full array BGA footprint and ample passive components in the package. Processes were developed to optimize assembly yield and package reliability, including an extensive board level reliability test. Assembly materials were selected to achieve excellent assembly yield, high thermo-mechanical reliability, and increased package functionality.

INTRODUCTION

High-end networking and computing applications drive silicon technologies for higher data rates and increased bandwidth. The greater functionality and processing speeds required of today's networking ASIC's have driven flip chip packaging technology into much larger sizes and increased I/O count with ultra low K Si, high substrate layer count, fine pitch Cu Column bump, and thin package/core thickness or even coreless

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substrate. All the listed parameters challenge existing packaging technology, materials, assembly capability, and 1st level and 2nd level reliability issues. In addition to assembly and reliability challenges, a significant investment of money, time and technology development is required. The objective of the study was to develop a robust packaging technology for a high I/O count, large flip chip package that can address all the requirements for high speed packages without compromising reliability and cost. In addition, the solution ensures there is no change in printed circuit board (PCB) design and cost. This study discusses various benefits of large packages, assembly challenges, detailed processes, and bill of materials (BOM).

PACKAGE DESIGN

In this device design, a 21X22mm die size with 16nm silicon was used with full array bumps at 150um pitch. The 50X50mm body size featured 0.8mm BGA pitch with over 3200 solder balls in a 6-2-6 layer substrate. A 400um thick substrate core material was chosen as low coefficient of thermal expansion (CTE) material to control the package warpage/coplanarity in addition to ELK die protection.

The package was designed with 0.4mm solder pad opening using 0.55mm SAC 305 BGA balls. A two piece lid with stiffener ring and flat lid was the preferred configuration for the flip chip package due to the significant number of passives in the package. There were approximately 19,000 Cu column full array bumps with 150um bump pitch and standard bump height with Cu pillar and SnAg solder cap. Overall, there were no issues for a standard gap height bump for the capillary underfill flow (CUF) process. Figure-1 shows the typical lidded fcBGA package structure.

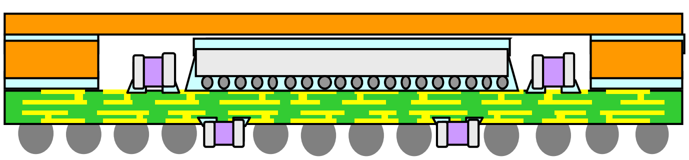


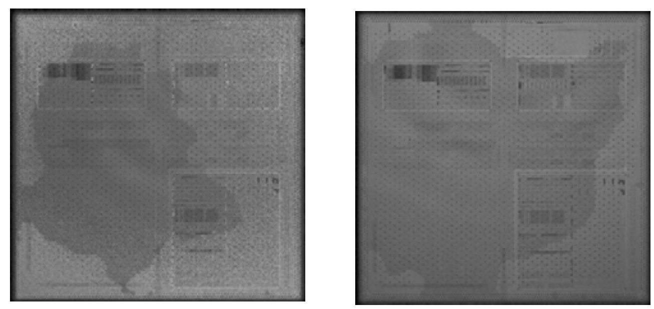
Figure 1: Typical large body lidded flip chip package with passives in both die and BGA sides

There were a significant number of capacitors placed on the die side and land side of the substrate. Multiple stack vias were used in the design with via on pad and bump on via configurations.

ASSEMBLY PROCESS

Packages were manufactured at several development phases described below.

Feasibility build: One of the critical phases in manufacturing was the feasibility build with the selected materials. Several key design parameters such as substrate core materials type, lid attach process, assembly process parameters, etc. were reviewed. A comprehensive DOE with assembly process parameters was conducted. Die ELK delamination and/or cracking were also concerns for 16 FF die with Cu Column and large die/large body size packages. In the assembly process typically Quick Temperature Cycle (QTC) test conduct to see the robustness of the Si structure especially for lowk or ultra lowk Si. The QTC test conduct for non-underfilled packages (righ after die attach process). A standard QTC consist of a profile at -40^{0}C to 60^{0}C with 4 minutes dwell and ramp. Figure 2 shows the results of a typical QTC test after 60 cycles for an ultra lowk die. No delamination or crack was observed in the die after 60 cycles.



0 cycle 60 cycle

Figure 2: Typical QTC results for an ultra lowk die

MATERIALS CHOICES

Package warpage is a big concern for large die, large body flip chip packages, especially those with thin core substrates. A low CTE core substrate is required for large packages with ELK die. Low CTE cores help mitigate "white bump" (WB) issues and reduce warpage by minimizing thermal mismatch between the substrate and die. In this study, a 14 layer substrate (6-2-6) with 0.4mm low CTE core was used. The substrate was designed with proper metal balance on each layer to minimize warpage and other potential substrate related failures in the package. Several iterations of the design and assembly process were performed to finalize the process window. A standard flip chip BGA device assembly process was applied in the study as shown in Figure 3.

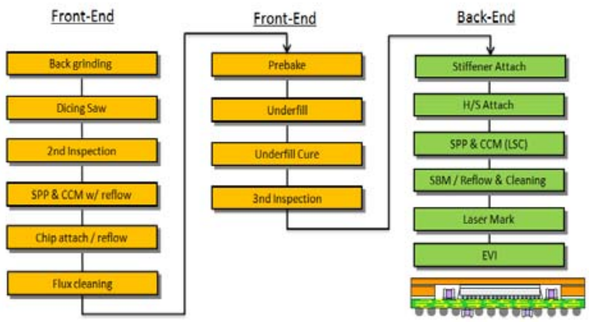


Figure 3: Typical assembly process flow for flip chip BGA

A comprehensive Design of Experiment (DOE) was conducted to study the warpage behavior of the package using various lids curing process. The warpage DOE description is shown in Table 1 along with room (25^0C) and high temperature (260^0C) warpage numbers. There was a very big difference in warpage between various cure process and stiffener attach at room temperature (RT), and at high temperature (HT). Additional DOE with assembly processes modifications were required in order to lower the package warpage at HT. Warpage for each leg was plotted against the temperatures shown in Figure 4. Bare die (no lid) condition package warpage is much higher than lidded conditions as shown in Figure 5. From the warpage study, the conclusion was the 1.5mm thick lid would be a better choice for such large packages. Additional study is needed to confirm the above statement.

Stiffener attach	H/S cure	Coplanarity (um)		Thermo Mori'e (um)			
				RT (25 C)		HT(260'C)	
		Avg.	Max	Avg.	Max	Avg.	Max
Standard process	Standard Cure	206.2	255	196	210	130	136
Pre-attach stiffener	Standard Cure	190.3	245	170	196	121	128
Standard process	Snap Cure	155.7	185	136	148	118	125

Table 1: Feasibility DOE package warpage data

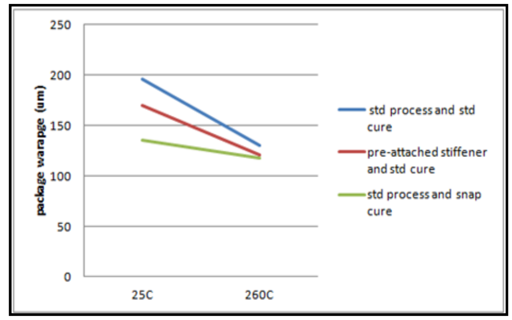


Figure 4: Package warpage against various process and lid attach cure conditions

NUMERICAL ANALYSIS

Prior to completing assembly and warpage measurements on the packages, a finite element analysis (FEA) was performed to better understand the underlying physics of the deformation patterns observed. A comprehensive new modeling methodology was developed and used in this case to understand the deformation seen on the package and die side for each assembly process step: chip attach, underfill dispense and lid attach. An illustration of the FEA model is shown in Figure 5.

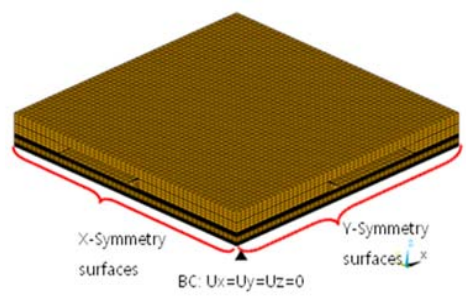


Figure 5: Typical Quarter Symmetry FEA model

To simplify the simulation, quarter models were constructed for all the legs with 3D linear elements. The package's stress free temperature is assumed at 150^0C which is the underfill's curing temperature. Substrate core thickness plays a significant role in controlling the package warpage. Typically much lower package warpage observed with a lower CTE core substrate. In this simulation study various core thickness along with two different build up materials were incorporated to understand the package warpage trend. Table 2 shows the warpage simulation results for core thickness and build up material type at various temperatures. For the package with 400um core, the experimental warpage at room temperature is around 150- 180um, while the simulated warpage is around 113um. A thicker substrate usually makes package warpage much lower which was observed in the simulation legs below. A big discrepancy was found in high temperature warpage. The discrepancy of warpage in between simulation and experiment is likely due to the material nonlinearity and processing factors which were not properly incorporated in the model. An illustration of leg #1 package warpage at 25^{0}C is shown in Figure 6. More warpage and a CPI study with a fine tuning of the FEA model will be conducted for next generation package development programs.

Leg #	Build Up Material	Core Thickness	Package Warpage (um)			
			25C	100C	220C	260C
1	G1	400um	113	38	-49	-47
2		820um	80	27	-36	-33
3		210um	140	44	-58	-54
4	N1	210um	131	45	-67	-109

Table 2: Warpage simulation results with various core thickness and build up material types

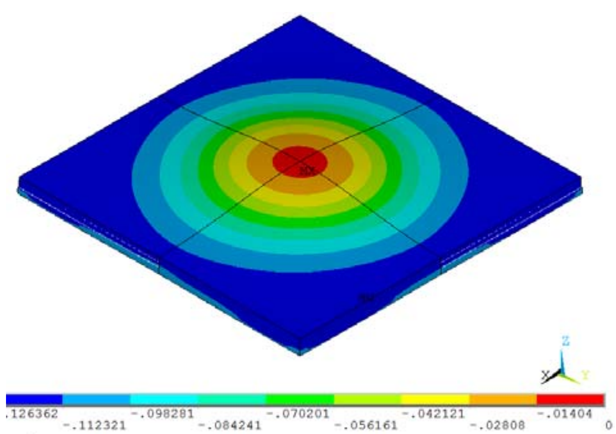


Figure 6: Package warpage data (leg#1) at 25^{0}C

PASSIVE AND LID ATTACH PROCESS

There were total of over 240 passives mounted in the package. As stated before, both die side and land side passives were used in the package. Placing the capacitors directly under the die perimeter was chosen because it is believed to be the highest L2-interconnect stress zone. Determining the reliability impact removing BGA balls (from the under die perimeter area) will have on the adjacent BGA balls is essential in understanding how far BGA-capacitors can be placed away from the zero-stress point (center). The gap between nearest passive to BGA pad is very challenging. In this design the smallest gap identified was a few hundred microns. Figure 7 shows how densely the passives were placed on the BGA side of the package. Typical passive heights were as low as 200um.

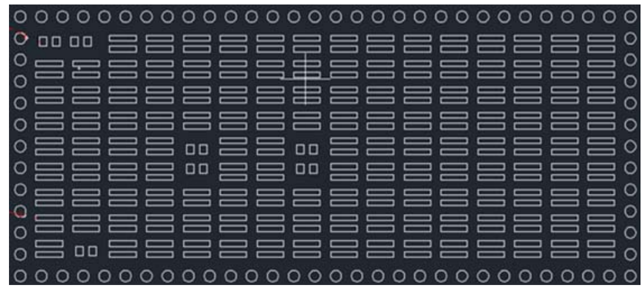


Figure 7: Typical picture of land side passives pad in large flip chip package

Lid attach is another challenging area in the large package assembly process. Special attention is required to develop the right dispense pattern for thermal interface material (TIM) and adhesive. A typical “X” type dispense pattern on the die backside with supplier recommended cure profile was been applied in the assembly process shown in Figure 8 below. A standard snap cure lid attach process which is integrated with the flip chip line was used in the assembly process. Silicone gel based soft Thermal Interface Material (TIM) with high thermal conductivity was selected in the DOE. The standard process was followed to detect TIM and adhesive coverage in the assembly process. Lid pull tests were performed after end-of-line (EOL) for all legs to make sure lids were attached properly and maintained certain adhesion strength. Both TIM and lid adhesive materials were extensively characterized to meet certain requirements such as wider process window to dispense epoxy and attach lid, higher lid-pull strength, low thermal resistance, etc.

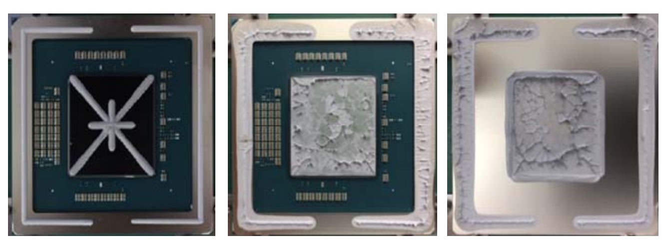


Figure 8: Typical TIM and adhesive dispense pattern

Several other process parameters such as with and without chemical for DI water clean and underfill volume (±10% of process of record) were also considered in the feasibility build DOE.

Selecting the right underfill material for large flip chip packages is always challenging. A large die package requires high Tg (glass transition temperature) underfill to protect the bumps from CTE mismatch. On the other hand, high Tg underfill creates more die or ELK stress in the assembly process. There is a tradeoff between die or ELK stress and bump protection. Moreover, high Tg underfill will create high package warpage or coplanarity. In this study a moderate Tg underfill was selected in the feasibility build to fulfill the package needs. A combination of “I” and “U” pass dispense was used to make sure no underfill voids and underfill bled out or creep occurred in the die. Since there were a large number of passives between the die to package edges, extra precaution was taken to make sure no passive touched the underfill. Figure 9 shows the passives in the die side along with a very tight underfill bleed out.

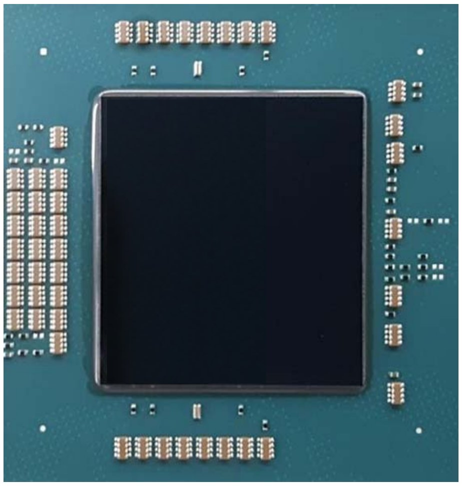


Figure 9: Representative picture of underfilled die and passives with very small underfill bleed out creeping

A check list for various process steps was monitored during the assembly process to ensure it met all required conditions. The detailed check list with monitoring methodologies is shown in Table 3.

Electrical open short (O/S) tests are performed after each accelerated test condition. Any failed unit is cross-sectioned to verify failure results and failure mode.

Recently a 3rd feasibility build (shown in Figure 10) was completed to further understand the warpage behavior of the package and determine how we could improve the package warpage. .A manual lid attach process was used in the recent build which seems to be a big factor for higher package warpage. A fully automatic snap cure gang press lid attach process will be used in the upcoming DOE. Based on the prior experience on large body flip chip package, the adhesive pattern seems to be another area to improve package warpage. Other areas for warpage improvement will be investigated including adhesive pattern and other TIM and adhesive options. A separate study has been recently conducted on a different package size with two types of adhesive dispense pattern (“C” and “2U”). Results show that “C” dispense pattern is better for package warpage (shown in Table 4). Further study with fine tune assembly process is needed to improve the package warpage (< 150um at 25^{0}C).

Process	Check Point /Methodology	Check Items
DP	Visual / optical Inspection	Sawing quality, Die chipping, Kerf width, Wafer Crack, solder void, bump shear
SPP/CCM	Visual Inspection	Paste wetting, Mis-placement, Tombstoning
FCA	Die peel	Flux Residue, coverage , Bump Joint
	X-ray	Alignment, Bridge , Cold Joint, Bump Void
UF	Visual Inspection	UF Bleed-out, Fillet Height/Coverage Creeping on die, UF crack
	C-SAM	Void , Delam, Bump/IMC/Pre-solder crack
LDA	Visual Inspection	Placement Accuracy, Bleed-out, BLT
	Lid pull	Adhesive strength
	C-SAM	TIM/Adhesive void, coverage
SBM	Ball Shear	Ball Shear Strength
	X-ray	Solder ball void
BE/EVI	AOI POD compliance	Coplanarity, Dimension, construction analysis, HT Warpage
Reliability Test	C-SAM / X-section	Delamination / white bump / bump & pre-solder crack

Table 3: Checklist for assembly and reliability

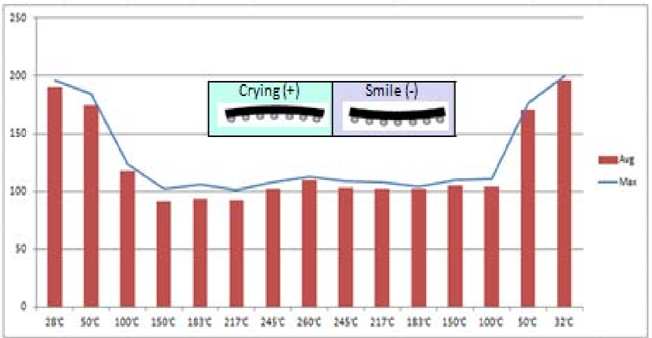


Figure 10: 3rd DOE build package warpage data

Leg#	Underfill type	Adhesive pattern	Thermo Moir'e data	
			25^{0}C (um)	245^{0}C (um)
Leg 1	UF A	"C"	105	-157
Leg 2		"2U"	139	-181

Table 4: Effect of adhesive dispense pattern onto package warpage

As of now, only the feasibility build has been completed for the program. After the feasibility build validation, the build DOE will be conducted to make sure no variability in the assembly data prior to qualification build. A validation build is also referred to as pre-qualification build. One leg with the best process and BOM will be selected for the build. Full JEDEC reliability with a smaller sample size will be used in the validation build. Table 5 described the validation build DOE BOM

wafer	substrate	core	underfill	TIM	adhesive
full loop	6-2-6L	E1	UFA	TIMA	AdA

Table 5: Proposed validation builds DOE

FUTURE WORK

More DOE will be running with various assembly processes to minimize the package warpage at room and high temperature conditions. After successful completion of feasibility DOE, the project will enter into validation build and finally a qualification build with JEDEC standard full package level reliability tests. A comprehensive failure analysis will be conducted for each failure or abnormalities during assembly and reliability tests.

Proposed Qualification Build

The leg with the best result from the characterization build will be selected for both package and board level qualification. Packages will be built with 3 different lots. If no noticeable issues are observed in the package assembly process, CSAM results will be taken on every part after the underfill cure process to make sure no underfill voids or delamination occurred in the packages. Package level post reliability requirements are kept the same in the qualification build (JEDEC standard package level reliability tests: preconditioning with MSL-3, uHAST, HTS, and TCB). The detailed test matrix (3 lots or 3 legs) for the package level qualification build is shown in Table 6. Again, electrical open short tests will be performed on every part after every read-point. A detailed reliability condition along with sample size is shown in Table 7.

leg	substrate	core	underfill	TIM	adhesive
leg1	6-2-6L	E1	UFA	TIMA	AdA
leg2	6-2-6L	E1	UFA	TIMA	AdA
leg3	6-2-6L	E1	UFA	TIMA	AdA

Table 6: Package level qualification builds DOE

Test		Conditions	Duration	Response	
				E-Test	CSAM
Assy process	warpage	Max 150um at HT			
	lid pull	Room and High temperature conditions			
Package Reliability	QTC	-40 to 60C; CSAM after 10X, 20X, 30X, and 40X			yes
	MSL3	30C/60% RH, 260C peak		yes	
	TCB	-55 to 125C	300/500/1000X	yes	
	uHAST	85% RH/130C	100 hrs	yes	
	HTST	150C	500/1000 hrs	yes	

Table 7: Package level reliability requirement

Once comprehensive reliability testing is completed on the qualification build samples (and samples pass), the process will be ready to scale to high volume manufacturing. Typical reliability read-points for the qualification build are EOL, X-ray inspection, CSAM to check for any voids, delamination or other abnormalities during assembly and accelerated test conditions, and package warpage as a function of temperature. Electrical open short testing will be performed after each test item using a dedicated high volume, fully automated, test socket. Extensive failure analysis will also be conducted to monitor material interface delamination, cracking, or any other abnormalities in the package.

CONCLUSION

Continuous trends in die and package size increases, performance improvements in node reduction, and the resultant move to ELK dielectrics have created the need for a robust process and BOM for large flip chip packages. The large die large package flip chip technology evaluation for high speed application is really a challenge in the assembly industry. With the selection of proper BOM and assembly process, a package can comfortably manage all critical JEDEC level reliability tests and assembly yield.

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